

5.02 Removing Modules

Remove the 2 module retaining screws, located at the top and bottom of the module, and carefully remove the module using the module lifting tools provided, the holes for the tool are located under the magnetic scribble strips.

The module will still have some cables attached, these will be the 10-way IDC and the two method connectors located at the top of the module. The cables attached should be long enough to remove the module.

An extender PCB can now be plugged between main 64-way IDC on the mother board and the module.

Although damage to the module will not be caused by plugging and unplugging the module with the power still switched on, this is not recommended for the inexperienced, as it is possible to bend the connector pins if care is not taken.

When replacing the module the 64-way connector should re-locate into the mother board.

5.03 Removing Patch Cards

The entire patchbay is made up from rows of plug in patch cards, constructed with printed circuit mounting jack sockets. Each row can be easily removed for cleaning and replacement if this should prove necessary.

To remove the whole patchbay assembly unscrew the 6 patchbay retaining screws, located at the top and bottom of the patchbay. This will allow the whole assembly to be lifted up and tilted to one side. Take care to avoid scratching the paint.

Since it is not often that you would wish to remove the whole patchbay the patchbay is also split into sections containing I/O patchcards, Command Module patchcards and tielines. To remove any of these sections simply unscrew the 4 retaining screws located in the corner of each section.

Having lifted out the patchbay, or part of the patchbay, locate the card which is to be removed and unplug the ribbon cables connected to it, and, if necessary, the adjacent cards. Remove the two screws holding the card to the panel and withdraw the card from the assembly.

Reassembly of the patchbay is the reverse of the above procedure.

5.04 VU Meter Alignment

The master VU meters are driven from the PCB below the meters which contains the phase correlation meter. The potentiometers

to adjust these meters are located as shown in Fig .

0VU is normally adjusted to indicate a line level of +4dBu, ie. a level of 1.228volts. However, it can be readjusted to indicate a different line level if required by the preset potentiometer on the drive card.

Connect a millivoltmeter to the output of the console. Route the oscillator set to 1kHz to the Mix bus by selecting 2T on the oscillator section of the Command Module. Adjust the Mix output level to read the required level on the millivoltmeter. (Normally this would be +4dBu.) Adjust the VU drive preset to indicate 0VU on the VU meters.

5.05 Lamp Replacement

To replace the lamps first remove the cover on the back of the meter bridge by removing the retaining screws located at the top of the cover. The lamps are located on top of the meter and may be removed by removing the retaining screws which hold the backplate of the bulb holder to the meter bridge. The bulbs simply clip in and out of the bulb holder.

5.06 LED Metering

The LED display consists of 30 segment bargraph metering, grouped into sets of eight, and 8 rectifier sub-PCBs.

The Meter rectifier PCB takes a signal input and converts it into a DC voltage that is used to control the bargraph circuitry. This card operates in either VU or Peak mode.

CALIBRATION

Calibration is normally done by setting the VU sensitivity first:-

Connect a millivoltmeter to the output of the console. Route the oscillator set to 1kHz to the group outputs by selecting 24T on the oscillator section of the Command module, adjust the level of the group output to read the required level on the millivoltmeter. (Normally this would be +4dBu.)

Preset PR1 is set to illuminate the first red LED, (=0VU), at a level of -2dBu. Note that this corresponds to an output from the balanced O/P stage on the I/O module of +4dBu.

The Peak mode drop is set by preset PR2 and is normally set to -8dB, although the available range is -3dB to -13dB.

NB: Early TS24 models were fitted with an earlier model rectifier PCB (SC1398), not fitted with a Peak-drop trim pot.

The presets are located on the Meter Rectifier PCBs and are obtainable by removing the meter bridge cover.

5.07 Power Supply Servicing.

The TS24 large Power Supply Unit provides the following regulated supply rails are provided;

- i) +/- 17 volts, Audio
- ii) +/- 24 volts, LED meters
- iii) + 48 volts, Phantom Power
- iv) +/- 7.5 volts, logic

If a power supply fault is suspected, first ensure that it really is the P.S.U. which is at fault, and not a short circuit in the console. This can be checked by disconnecting the P.S.U. from the console, and measuring the voltage at the connector. A load across the supply should be provided, to simulate the normal load conditions imposed by the console.

A 10 Ohm, 20 Watt resistor across each of the audio supply rails and a 20 Ohm, 5 Watt resistor across the +24 volt rail is suitable. The phantom power supply can be loaded with a 2.2kOhm, 1 Watt resistor.

The ripple and noise value of the various supply rails can now be measured, using a millivoltmeter or an oscilloscope, and a value of at least -80dB, (ref 0.775V, DIN audio should be obtained on the audio), on the phantom supply rails.

If a fault is found to exist in the P.S.U., disconnect the mains supply and remove the cover. Check visually for any obvious problems, such as blown fuse, burnt components, etc. If nothing obvious is observed, reconnect the mains and measure the voltages across the various electrolytic smoothing capacitors, which should be as follows;

Audio Supply	C1,C2	= +26volts
	C4,C5	= -26volts
+24volt Supply	C31,C35	= +36volts
Phantom Supply	C39	= +59volts
Logic Supply	C23	= +13volts
	C27	= -13volts

Differences of +10% are acceptable, due to variations in the incoming mains voltage. If satisfactory, the problem lies in the regulator section. If not, however, check the bridge rectifier, smoothing capacitor and transformer for failure.

6.00 GLOSSARY OF TERMS USED

AFL	After fade Listen: This button will "solo" the signal (or ALL with their AFL buttons down) on the monitors, and the feed for this solo is taken AFTER the fader.
Attenuate	To reduce the electrical level or amount of gain.
Auxiliary Send	Extra output from the console, usually used for echo sends and foldback.
Bus	Wire carrying a signal or sum of a group of signals.
Cold	The negative going current of a signal. With 2 signal wires, one is positive going (hot), and the other is negative going.(cold)
Cut	To cut a channel means to turn it OFF.
dB (decibel)	A logarithmic ratio used to represent voltage or power gain. The reference about which the ratio is made is usually stated.
Ground	Earth or screen of a cable when refering to connecting leads.
Group Output	The output of a group bus which is carrying a sum of all the signals assigned to that group number.
Hot	Positive going current of a signal. With 2 signal wires, one is positive going (hot), and the other is negative going.(cold)
Hz	Measurement of frequency (Hertz) 1Hz = 1 cycle per second.
Insert	An insert point allows peripheral equipment to be introduced into the signal path.
Khz	Measurement of frequency expressed to the power of 1000.i.e. 1Khz = 1000 cycles per second.
KOhm	Measurement of electrical resistance expressed to the power of 1000.i.e. 1 KOhm = 1000 Ohms.
Mains	Local Electrical Supply.
Multitrack Logic	Either the multitrack machine's monitor switching or its safe/record switching.

Ohm	Measurement of electrical resistance.
Overdubbing	The process of recording new tracks on a multitrack tape recorder whilst listening back in synchronisation with previously recorded tracks.
Pan Pot	A pan pot places a signal across two stereo lines (left & right) turning it to the left will send all the signal to the left line, and to the right, all of the signal will be sent to the right side. If the pan pot is left at its centre detent, an equal amount of signal will be fed to both sides and the image in the stereo picture will be central.
PFL	Pre fade Listen: This button will "solo" the signal (or ALL with their PFL buttons down) on the monitors, and the feed for this solo is taken BEFORE the fader.
Phantom Power	A voltage (usually +48 Volts) across the microphone input to power capacitor microphones.
POST	Post means after the fader.
PRE	Pre means before the fader.
Ring	The connecting part in the middle of a stereo jack, (it mates second).
Signal to Noise Ratio	The ratio between the level of signal and the level of unwanted noise.
Sleeve	The connecting part of a stereo jack which mates last and is always earth.
Star Point	A single point to which ALL earths are separately connected.
Sync	Used whilst overdubbing; previously recorded tracks are played back through the record head whilst you record on other tracks.
Tip	The connecting part at the end of a stereo jack, (it mates first).
Track Bouncing	Taking a group of previously recorded tracks and recording them as a group onto another track. e.g. bouncing down 4 vocals from 4 tracks to just one track "frees" 3 tracks for fresh recording.

7.00 TS24 IN-LINE MIXING DESK TECHNICAL DESCRIPTION

This description covers the standard I/O and Command modules of the TS24, including the following PCB's and circuit diagrams:

Circuit board	PCB no.	Drawing no.
TS24 I/O module Left-hand PCB	SC1516	ED2220
TS24 I/O module Right-hand PCB	SC1519	ED2219
TS24 Command LH PCB	SC1420	ED2159,2160
TS24 Command RH PCB	SC1394	ED2156,2157
I/O Module Block Diagram		ED2158
Command Module Block Diagram		ED2161

Operating Levels

The TS24 operates normally with standard +4dBu input and output levels. However, the internal operating levels are reduced to a nominal -2dBu, giving 6dB greater headroom. The use of advanced circuitry means that the noise performance of the desk remains very good. The only significant consequence of this reduced internal level is that the insert send/return points are at -2Bu: all other ins and outs are at +4dBu.

In addition, the "2-track C" replay input can be configured to match -10dBV (-7.8dBu) TASCAM operating levels, for ease of use with cassette machines, etc.

I/O Module Description

The circuitry of this module is divided between the LH and RH boards, with both audio and logic signals moving between them, and it is not normally possible to carry out functional checks of the module without the two boards being connected by the three 10-way interboard IDC cables.

7.01 Left-hand PCB

Signal Stages

The LH board carries the following signal-handling blocks, in addition to almost all the module logic functions:

Input Circuitry. (Pads, phase switch etc).
Insert-send ground-cancelling (GC) O/P stage.
Insert-return balanced input stage.
Group summing amp.
Balanced O/P stage. (See O/P to multitrack).
Group-monitoring balanced-input stage.
Tape-return balanced-input stage. (ie. multitrack return).
T and G buffer. (See below).
Aux signal selection (eg pre/post fade).
Routing matrix and track bounce switch.

The Module has two inputs. The channel input serves for both normal low-Z mic and balanced line inputs, with a selection of the function at any given time being made at the patch-bay. The D/I switch on the module (S2) switches in and out two separate attenuator circuits, both of which are controlled by the 4-pole PAD switch S3. The mic side has a standard low impedance 15dB pad, with the usual phantom-power arrangements at the input end; C18,19 keep the +48V out of the rest of the mic circuitry. R140,141,142 define the input impedance for the mic input. S4 is the phase switch (active in both mic and line modes), which simply swops over the two balanced inputs. The Line/DI attenuator, (R59-62), operates at a much higher impedance, to prevent undue loading of guitar pick-ups, etc, and has an attenuation of 30dB. From S4 the balanced input signal goes to the input pre-amp on the RH board.

The insert-send GC O/P amplifier, (IC30A), is a single-ended, (non-balanced), stage that nonetheless has the capability of allowing connection to external grounded equipment without introducing ground-loop hum. Briefly, the normal output is at low impedance via C15 and R52, and a normal ground is also available at Conn F. The third wire, going to R49 and R53, is infact an input rather than an output, and in effect this samples the ground of the external equipment, and any spurious noise or hum is then added to the GC output signal in such a way that as far as the external equipment is concerned, the signal is clean. R48,49 attenuate the signal coming into the stage by 6dB, and perform the summing. R50,51 define the op-amps gain as +6dB, giving unity-gain overall for the GC stage. The insert-send signal goes to the patchbay via an IDC cable, and is there normalled through to the insert-return input on Conn F if no jacks are inserted.

The insert-return amplifier is a completely conventional differential op-amp stage, (IC3-B), with unity gain. S12 is the INS switch; with this released the state of the patchbay is irrelevant as the insert point is completely by-passed, signal flowing through S12-B while S12-A grounds the other leg of the balanced input amp; however, a GC output is still available for Direct Out purposes.

The group summing-amp, (virtual earth mixer), is IC1a. This is a fairly conventional shunt-feedback stage with a few improvements. R27 takes care of the DC feedback, while most of the AC feedback is via R28. The amount of feedback can be varied by VR1, the Bus Trim control. Thus the gain of the stage, (with a 22K mixing resistor as input), may be varied between +8dB and -10dB, allowing overload problems to be dealt with at source, rather than having to pull down all the faders feeding that group. R29 adjusts the law of the control to give 0dB gain at the centre-detent of the control.

The electronically-balanced group-output stage is built around IC2. This op-amp has a combination of positive and negative feedback applied to it such that it simulates the action of a floating transformer winding; if either output is grounded the other increases in level by 6dB to give a constant voltage across the output terminals. Note that this stage must be balanced by use of the preset control VR2, so that the output amplitudes are equal with no loading. This can be simply done by connecting two resistors of known equal value to the outputs, and joining the two free ends together. The preset is then adjusted to give a voltage null at the junction point, and no accurate measuring equipment is therefore necessary. This adjustment is done at manufacture and should only need alteration if either of the SIL resistor packages are changed. Changing the op-amp should not affect the calibration.

The balanced line-input amp for the group monitoring is IC1b. this converts the signal to a single-ended form, and provides an attenuation of 6dB to reduce an incoming +4dBu to the TS24 internal operating level of -2dBu.

The tape-return balanced input stage is built around IC4-A. This is a conventional differential amplifier with a nominal output level of -2dBu. The output of this stage is one of the few places in the I/O module where the signal is out of phase.

The T&G, (tape and Group), buffer selects the correct input for the mix signal path; this is normally either the group-output, (signal to multitrack tape machine record inputs), or the tape return. (Multitrack replay outputs). The correct input is selected by the two junction FET's Q7 and Q8, which are controlled by the I/O module logic, in such a way that one FET is always on, and the other off, forming an electronic single-changeover switch. When an FET is off, the voltage on its gate is taken down to -22V, via D1 or D2, and the resistance

between the source and drain, (these two terminals are effectively identical in this type of FET), goes very high - in the region of tens of meg-Ohms, and no signal passes. When the FET is on, the voltage on D1 or D2 cathode is taken up to +16V, and the diode ceases to conduct. However, the voltage on the gate must now be defined as nearly equal to that on source or drain if low distortion is to be achieved, and this is done by bootstrap resistors R46 and R47. Note that R47 is connected to the op-amp side of DC-blocking capacitor C2, so that current can flow freely through it when Q8 is biased off. R42 is a loading resistor that minimises the effect of capacitative feedthrough of transients from the FET switching signals.

In RECORD mode, Q8 is on so that the group-monitoring balanced-input amp signal is sent to the mix path when the monitor path is thus set with "Group" as its source. The signal is taken from the patch-bay, from where it is taken AFTER the group insert. Hence if the group signal undergoes any processing, (eg. compression), before being sent to tape, then this is reflected in the monitor signal. Since the signal at the group insert is balanced, an additional balanced line-input stage is required, (IC1b).

In MIX mode, Q7 is on, the multitrack tape replay signal is used instead. However, when the T & G switch S27 is pushed in, the FET switching system is by-passed, and the T & G buffer, and hence the rest of the mix path, is fed with the sum of the tape replay and the group signals. This mode is used for overdubbing. The summing is performed passively by resistors R39,40, and 41, the sum signal being selected by S27-A; R39,40 are counterpart of R41, the resistance being split into two sections so that the group signal can be disabled when the FDR switch is in use. The reason for this is explained later.

In T & G mode, the meters read the group signal at its full level, rather than the sum; this is taken care of by S27-B. S27-C ensures that the tape/group logic is always reset to TAPE when the T & G switch is released, as this will normally be the next mode required. S27-D causes the tape-group LED to flash rather than show a steady state, to indicate that a slightly unusual state of affairs exists. The action of this logic is explained below.

From the tape/group switching system, the mix signal enters the T & G buffer itself; this is an inverting (virtual earth) stage in order to restore the phase of its output signal. The Line-Trim gain-control is built around T & G buffer IC4b. The second section of VR1 controls the feedback around this stage, via R45. The maximum gain is set by R44, and C35 ensures 100% feedback at DC to minimise offset voltages; the gain range is from +8 to -10dB. Tapes recorded at non-standard levels can therefore be accommodated.

From the T & G buffer the Mix signal passes to the RH PCB via Connector C, the lowest of the three interboard connectors.

The aux signal selection on the LH PCB consists of the switches S5-S10. For each pair of auxes, (1-2,3-4,5-6), the feed may be selected from either channel or mix paths, pre or post fade in each case. These four signals reach the selection switches via the top inter-board connector.

The routing matrix takes left and right signals from the channel pan buffers on the RH PCB, and sends them to the appropriate group virtual-earth buses via 22K mixing resistors. Note that the switch is on the bus side of the resistor, allowing the signal to be grounded by the back-contact when it is not routed to the bus, and so preventing capacitative cross-talk across the switch. The channel signal may also be routed directly to the Mix L and R buses, but the routing switch for this is on the RH PCB.

It is frequently convenient in multitrack work to route a channel to its associated group and no-where else. This may be done via the Direct switch, S25. When this is pressed, the channel postfade signal is routed directly to the group sum amp via mix resistor R26, which is otherwise grounded by the back-contact of S25-A. Simultaneously, S25-B disconnects the mix bus from the sum amp and grounds it to prevent crosstalk if other channels are accidentally routed to this bus.

Normally the routing matrix is fed with the channel pan signals, but this is not always the case. The BNC, (Bounce), switch S29 allows simple track-bouncing as follows. When it is operated, S29-C,E remove the channel signals from the matrix, and S29-D,F replace it with the mix pan-buffer signals. At the same time the mix signals are removed from the path to the mix bus, which is normally via R70,71. This a sub-mix which has been balanced satisfactorily on the mix long throw faders can be transferred at once to any selected pair of tracks without having to try and duplicate this balance on the channel rotary faders.

Left-hand PCB logic circuitry

The LH PCB carries all the logic, FET drivers, and electronic status display circuitry. The functions may be summarised as:-

- Control of EQ flip, (ie whether the EQ is in channel or mix).
- Control of the group/tape switching for the mix path.
- Control of the CUT function and muting.
- Control of SOLO and PFL/AFL functions.
- Current source for LED ladder.
- Initial reset and power-supply for local logic as above.

The EQ block, which includes the HP filter and the insert point, is flipped, (ie moved bodily from the channel path to the mix path), by means of 6 FET switches on the RH PCB. These are under the control of flip-flop IC5-A,B, which may be changed in state either locally, (using FLIP switch S11), or centrally, for all I/O modules at once, from the Command Module. At power-up it is reset from the command module so that the EQ is in the mix path. (FLIP LED off). This corresponds with a logic high at the output of IC5-B.

In this state, C26 charges high through R79; the flip-flop is latched by positive feed-back through R78, which applies a low to IC5-A. When S11 is closed, the charge on C26 momentarily overcomes the effect of R78, and the state of the flip-flop reverses. If the switch is held closed, or closed again very quickly due to contact bounce, no further flip occurs as C26 has had no time to re-charge, and R78 overpowers the direct effect of R79. Only after a short period with S11 released can another flip be initiated.

The MODE line applies a DC control voltage from the Command Module, indicating whether RECORD or MIX is the current central mode. A third mode, (TV), is possible using the TV control line; this will be explained in a separate section below. The MODE signal is only applied to the flip-flop when the CHG, (change), control line goes high to signal that a central command is being given; when this occurs analogue gate IC7-A conducts and the MODE line forces the flip-flop into the current state. For the rest of the time, the flip-flop may be freely locally flipped. R76,77 are protective resistors that allow the CMOS protection diodes to absorb transients on the control lines without damage. R80,81 take complementary outputs from IC5, and apply them to FET drivers Q1,Q2, which provide switching voltages swinging from -22 to +16V, to 4 of the 6 EQ-flip FETs. (F2,F3,F5,F6 on RH PCB). The remaining two are driven from Q10,Q11 to allow over-ride by the TV mode. The MODE line also switches Q3,4 in antiphase; these drive F10,11 on the RH PCB to select the PRE fades from either before or after the electronic mix-path mute, depending on whether the central status is RECORD or MIX. The status of the EQ flip is shown by LED2, controlled by Q20.

A second flip-flop, (IC5-C,D), controls the group/tape source switching in a similar way. S28 is momentarily closed for a local flip of status, using the charge on S27; Q5,6 are the drivers for F8,7. The central control lines operate slightly differently; a low on the GRP line, for example, forces a read-group state, and likewise for tape. R89,90 are protective resistors, and IC7-B provides a lockout to prevent confusion if both commands occur at once; IC7-B is normally controlled from the TPE, (tape), line, and switches off when TPE is low, blocking any GRP signal. S27-C,D provide the T & G mode; S27-C, when operated, disconnects the TPE line and disables the GRP line by forcing IC7-B off, rendering the flip-flop immune from central status changes. This switch also ensures, by grounding

R91, that the flip-flop will be in TAPE mode when the T & G switch is released. S27-D disconnects the SRC, (source), LED control transistor Q21 from the flip-flop and instead drives it from the flash bus, which carries a 2Hz sinewave.

The CUT and SOLO flip-flops both work in the same way as the two described above, except that essentially only local changes of state are possible. The module applies a local initial reset on power-up so that CUT and SOLO functions are both off.

CUT is controlled by IC6-A,B, which may be flipped by the momentary illuminated switch at H6,7. The output of IC6-B is low when the mix is CUT, but a CUT may also be applied by the mute buses A and B, via S31,D5 and S32,D6; the mute buses go low when asserting a CUT so normally D5,6 do not conduct. A cut may also be forced regardless of the state of the CUT flip-flop by D10, which allows muting during solo-in-place.

From this point, R108,109 drive Q12, which provides level-shifting for the mute drive system. The mix mute itself, (RH PCB), requires carefully timed antiphase drive signals to the two FETs involved; basically the drive voltages swing from -22 to 0V, and are controlled by R111,D7 and R118,D8 so that both go up quickly and down slowly. C29,30 provide the timing of the soft-mute, and Q14,15 drive the bulb in the CUT switch. R121 keeps the filament dull red when the bulb is nominally off; this allows the switch to be located in the dark, and extends bulb life.

The solo function is controlled from the flip-flop IC6-C,D. This can be locally flipped by means of the push-switch at H2,3. The output of IC6-D is high when a solo condition takes place, and Q16 switches on the bulb at H1,4 to display it. This may, depending on the setting of two switches on the command module, represent a PFL, AFL, or solo-in-place, (SIP), facility. In the first two cases, the SOLO switch lights and signal is routed to the PFL/AFL buses, but no interruption of existing signal paths takes place. In SIP, all modules without their SOLO switches active are muted centrally from the command module, leaving only the channel(s) of interest operational.

The SOLO state is signalled to the command module via the solo-enable, (SEN), bus; this has three possible states, represented by logic high, (SIP/PFL/AFL depending on command switches), logic low, (always PFL/AFL), and a voltage mid-way between the two. (SOLO facilities inactive). The first of these sends is signalled from the SOLO flip-flop via D9 and R123. A complementary signal from IC6-C turns off IC7-D. This blocks the solo-mute signal, sent out by the command module in response to a high on the SEN bus, from turning off any module which has its SOLO light on. This solo-mute is normally applied as a high on the SMT bus, turning on Q18 and enforcing a cut through D10. It is often desirable to separate an I/O module from the SIP system, for example to allow effects returns to continue to operate; this is done by using the SAFE switch S30,

which when operated disconnects the SMT bus from the logic.

The power supply arrangements are as follows. The CMOS runs from a local, (one per module), 12V supply that uses the main -22V rail as its common. (Vss). Therefore, the CMOS top rail, (Vdd), is at about -10V with respect to the mixer ground. Note that all logic and switching functions use a separate ground, called 0V(L), to distinguish it from the clean signal ground. Note that the +/- 16V rails for the signal circuitry are separately decoupled for LH and RH boards; this is done by R72-75, and C20-25.

The CMOS supply is regulated by REG1, a 78L12 positive regulator; this also powers the electronic TV routing board if fitted. A few very early consoles used a 12V zener instead. The LED ladder is powered from a current-source Q19, to eliminate current transients from the power rails. This is biased by D12,13.

On power up, the CUT and SOLO logic must be locally reset to the normal state. R133,C32 generate an initial-reset pulse that is held low for a few milliseconds at power-up, and then goes high, (inactive). D11 ensures that this circuit will reset quickly on short power interruptions.

7.02 The Right-hand I/O PCB

The right-hand PCB carries the following signal-handling blocks:-

Input preamplifier

EQ block, including High Pass Filter

Aux sends and their ON switches

Channel rotary fader, post amp and pan buffers etc

Mix path, including electronic mute, post amp and pan buffers

Multi-point bipolar peak detector and LED

Miscellaneous LED indicator and PFL/AFL circuits.

The input pre-amp is a standard Soundcraft circuit, accepting balanced inputs via C1,2. D1,2 and D20,21 provide protection against input transients, particularly those caused by phantom power. TR1,2 form a differential pair with gain set by VR1, and IC1a performs differential-to-single-ended conversion, (phase summing). The op-amp output is monitored by the peak-detect circuit, via D13,14.

The EQ block, which moves as one unit between channel and mix when 'flipped' contains the high-pass filter, followed by 4-band EQ with a sweep top and bottom and two fully-parametric middles, and the insert point. The insert send and return amps are on the LH PCB.

The high pass filter is built around IC1b, configured for a gain of +6dB, which in conjunction with input attenuator R10,11 gives overall unity-gain. This approach ensures that the op-amp clips cleanly on overload. The filter -3dB frequency is set by VR2, and S1b allows the stage to be completely by-passed.

The EQ is in four separate circuit blocks. The HF shelving stage is built around IC2a,b. Feedback or feedforward is taken from around IC2b by VR3A, allowing boost or cut. C16,R21, and VR3B form a variable-frequency low-cut network, which ensures that feedback/forward is only applied at HF. R17,R20 define maximum boost/cut, and are buffered by IC2a; note that the values here are fairly critical and a wrong value may result in HF instability.

The two middle controls are fully parametric, with variable boost/cut, centre frequency, and Q, (band-width). They are identical except for component values, only the first is described. As in the HF stage, feedback/forward is taken from around the inverting stage IC3a by VR5A, and is applied to a state-variable bandpass filter, consisting of two integrators and an adder/subtractor, (IC3b,c,d), which allows the circuit to act only within a band of frequencies. VR5B sets the centre frequency of the filter, R29,R31 setting the maximum. VR4 controls the filter Q by varying both the input signal and the internal feedback. R25,R26 set the range of Q available.

The LF shelving control works in a similar manner to the HF stage, except that differing impedance levels mean that buffering of the feedback/forward signal is no longer needed. VR8B controls the low-pass network cutoff frequency, and R42, R45 and R102 define both the maximum frequency and the boost/cut range. These three resistors are again reasonably critical, and other values should not be substituted.

When the PEAK/SHELVING switch S12 is pressed in, the LF stage is converted to a low-frequency "sweep-middle" configuration that gives a peak/dip response rather than the Baxandall-type shelving. Q is set by the value of C41.

EQ IN switch S2b allows the whole EQ block to be by-passed, but the HP filter remains available. C22,23 block DC offsets. From here the signal proceeds to the insert point, and on its return is again monitored for excessive peak levels, (see PK DET 2), via D15,16.

The EQ block is flipped between channel and mix paths by FETs 1 to 6. When the EQ is in channel, (FLIP LED on), FET 1 routes the input pre-amp signal to the EQ, and the output from this is routed to the channel fader via FET 3. At the same time FET 5 is on to route the mix signal from the LH PCB direct access to the mix fader. FETs 2,4,6 are off, showing effectively infinite resistance.

When the EQ is in mix, (FLIP LED off), the situation is reversed, FETs 4,6 routing the mix through EQ and FET 2 giving the input signal direct access to the channel fader.

The Aux sends are arranged in pairs, each pair taking a signal from the LH PCB which has already been selected for pre/post fade, and channel/mix. The ON switches, (See S6), ground the aux mix resistors, R48,49, when they are not connected to the bus in order to prevent capacitive crosstalk across the switch contacts. Since the aux sends represent a heavy load impedance, the PRE feeds require buffering by unity-gain followers IC6a,b; this is not needed for POST feeds due to the greater current capability of the fader post amps. Note that R57,58 are essential to bias the op-amps when the switches feeding them are between contacts.

The rest of the channel path is now dealt with. From the EQ flip FETs, the signal passes through the FDR, (fader), switch S3d. This allows the channel signal being sent to the routing matrix to be replaced by a mix signal, which may be selected pre/post by S9. This facility allows, amongst other things, easy sub-grouping. However, it also means that care must be taken so that if the DIRECT switch is in use, group monitoring is disabled, as otherwise a feedback loop is formed around channel, group and mix which can have a destructive effect on loudspeakers. To prevent such a path being established, when S3 is in, S3c turns off FET 8 on the LH PCB, and S3d grounds the relevant T and G sum resistors. (See LH PCB description).

S5b is the channel CUT switch, which operates purely mechanically. Electronic muting is confined to the mix path. S10 is the fader-reverse switch; this allows the channel rotary and mix linear faders to be swopped in function, in case it is necessary to 'ride' a signal onto tape.

IC8a is the channel post-amp, with a gain of approximately 10dB, set by R62,63. VR9 is the channel panpot, R64,65 giving a compromise, (for mono/stereo), pan-centre drop of 4.5dB. The two signals from this are sent to the routing matrix via unity-gain pan buffers IC9a,b. R66,67 and MIX routing switch S11 give the channel signal direct access to the mix bus.

The rest of the mix path is as follows. From the EQ-flip FETs, the signal enters the electronic-mute block. IC7b merely provides phase-inversion to cancel that given by the actual muting stage IC7a. FETs 12,13 are driven in anti-phase by the system on the LH PCB, in such a way that as FET 13 increases in resistance and turns off, FET12, turns on to shunt the signal away from it and prevent excessive distortion. However, care must be taken that the two FETs do not turn completely on simultaneously, as this will cause the gain of IC7a to increase greatly, and give an audible 'chuff' of noise. This is the reason for the apparent complexity of the mute driver on the LH PCB.

FETs 10,11 select PRE feed from either before or after the mute circuit, to suit the central mode selected, (RECORD or MIX); note that the FET gate bootstrap resistors R70,73 are higher in value than usual, to minimise clicks caused by DC flowing through the on-resistance of the EQ-flip FETs.

FETs 9,14 switch appropriate PRE or POST signals to the PFL and AFL buses, allowing this function to be controlled by the SOLO flip-flop on the LH PCB.

IC8b is the mix post-amp, which is also configured for a gain of approx +10dB, by R77,78. The panpot and associated buffers work exactly as for the channel path.

The LED ladder crosses over from LH to RH several times, which can make fault-finding tedious, but it terminates in the peak LED, (LED 6), which is controlled by TR 4. Most of the LEDs are controlled simply by shorting them out when they are required to be off, but the channel PFL switch, S4a, also triggers the SEN, (Solo enable), line. As described for the LH PCB, the SEN line has three possible states; logic high for SIP, logic low for PFL/AFL, and midway for off. It is therefore arranged so that any PFL switch will override any number of SIP signals, by asserting logic highs through 100K resistors, and logic lows through 1K resistors. Thus when S4a is operated, TR 3 is turned on through R95, and the SEN line is forced low via R96. R94 ensures that the ladder always has enough voltage available to turn on TR 3.

The peak detector system, IC5b, will detect either positive or negative peaks at any of its three monitoring points. These points are all at very low impedance so that diode action cannot introduce any distortion. When any point goes excessively high on a positive peak, one of the diodes D13,15,17 conducts and the inverting op-amp input, which is normally held below the non-inverting input by its associated bias resistors, is pulled above it and the op-amp output pulses negative. Similarly, a negative peak will cause one of D14,16,18 to conduct and pull the non-inverting input down below the inverting input, so that once again IC5b saturates negatively.

When this occurs, D19 rapidly discharges C37, and the base drive is shunted away from TR 4, turning it off and illuminating LED 6. When the peak is passed, the op-amp saturates positively, and D19 is reverse-biased, allowing C37 to slowly recharge through R91. This gives the required fast-attack, slow-decay action.

Finally, it should be noted that all the NE5532 ICs run hot to the touch in normal operation. These chips also must be decoupled close to the power supply pins, (this is usually done with a 2.2uF electrolytic capacitor), and failure of this capacitor will result in poor distortion performance due to internal parasitic oscillations.

7.03 TS24 NON-LINE TRIM MODULE TECHNICAL DESCRIPTION

Refer to circuit diagrams ED2151 and ED2155.

This technical description confines itself to the differences between the original TS24 I/O module and the Line Trim module described earlier. These are:-

1. There is no "Line Trim" facility available on the original module, instead there is a 6dB PAD which may be switched into the Monitor path, around the T & G buffer.
2. When the monitor path is set with "Group" as its source, the signal is taken directly from the output of the group summing-amp.
3. The peak/dip switch on the Low Frequency is not available.

Technical details

6dB PAD.

On the LH I/O PCB, (ED2151), extra feedback can be applied via S26 and R44 to introduce 6dB of attenuation, to allow the replay of 'hot' multitrack tapes.

THE COMMAND PCB'S

The command module consists of two main PCBs, with the command functions split between them as follows:-

LH COMMAND PCB

Mix summing amps, insert send and return amps, mono sum amp
Mix and mono post amps and EBOS
Control-room (CRM) select matrix
Studio feed chain and EBOS
PFL/AFL sum amps and PFL/Mix CRM switching
CRM monocheck, DIM and CUT facilities
CRM and alternate (ALT) speaker controls and EBOS
Phones 1 selection matrix, post amps and EBOS
SIP/PFL/AFL detect system and indicators, & solo-mute driver
Switch-tuned oscillator with sine/square/pulse outputs
VLF sine oscillator for flash bus.

RH COMMAND PCB

6 aux-master summing amps, post amps, and EBOS, with AFL
Phones 2 selection matrix, post amps and EBOS
Talkback mic amp, 30Hz slate oscillator and switching network
Listen mic amp and switching network
Resistor array for slating talkback, listen and oscillator
Master status control logic and power-supply
Programmable mute bus drivers.

7.04 LH Command PCB Description

The circuitry on the LH PCB will be described in the order in which it is mentioned above. Much of the circuitry is in stereo, and all component references will be to the right channel, unless otherwise stated.

The mix sum amps are required to give a very good noise performance with a large number of mix resistors permanently routed to the bus, and are therefore of a hybrid discrete/op-amp form. Q7 is a low noise transistor operating in common-base mode, with feedback around it being provided by IC10A. C27 is a DC blocker that allows the operating conditions of Q7 to be set independently to those of the op-amp. R94 provides the op-amp with DC feedback, and C26 stabilises the loop at HF. R92 is the main negative feedback resistor, and generates a virtual earth on the bus in the usual way. R93 provides a small amount of DC feedback to prevent VLF instability. C34,36 keep power-rail noise out of the circuit; note that these are shared between the two channels. From the sum-amp the mix signal passes to the insert-send amp IC11A, which is a ground-compensated stage exactly similar to that on the LH I/O PCB; the insert-return balanced amp is also essentially similar. However, it is important to note that this insert point operates at a depressed level of -6dBu, (nominal), as a result of the 4dB attenuation introduced by the mix sum amp, in combination with the nominal

internal operating level of -2dBu. The purpose of this is to increase headroom, the sum amps being quiet enough to make this feasible.

The mix signal then encounters the mix master fader. This is unlike the I/O linear mix faders in that the 0dB position is at the top of travel, rather than 10dB down. The mix master post amp, IC13A, is therefore configured with a gain of +4dB, set by R107,108. The signal then drives an electronically-balanced output stage, (EBOS), that is exactly the same as that in the I/O module. From here the signal normally goes to the patchbay via the 40-way IDC, but when S31E,F, (oscillator to 2-track), is pressed the patchbay is instead driven with a balanced oscillator signal, so that external equipment can be lined-up without taking over the mix bus. S31C,D switch the mix meters to read the oscillator output instead of the mix.

A mono feed is derived from the two mix signals by summing amp IC14A. This has an attenuation of 3dB, so that uncorrelated left and right signals can be combined with a minimal level change. The mono fader post amp, IC14B, is an inverting stage to correct the phase, and the signal is then fed to a standard EBOS, and out to the patch via the 40-way IDC.

The control room monitor, (CRM), select matrix is based around IC15A; the whole system operates in a balanced mode, conversion to single-ended only occurring after selection switches S9 to S15. The switch-bank is interlocked so that only one input will be connected to IC15A at any given time. The op-amp works as a normal balanced-input amplifier, the switch-bank changing over the input resistors as required. Input resistors not in use are grounded by the switch back-contacts, to minimise crosstalk.

As usual with balanced-input amps, the input resistors partly define the overall stage-gain, in conjunction with resistors R143,144. All inputs are configured for a +4dBu level, but 2-track C may be altered to deal with -10dBV, (Tascam), or domestic cassette levels by adding resistors R134,135. (And, ofcourse, also R163,164 in the left channel).

From the CRM-select matrix, the signal passes to the studio-feed chain and the PFL-switcher. The studio level is set by VR4, and passive mixing resistors R154,155 allow the talkback signal to be mixed into the studio feed when the appropriate FETs on the Command RH PCB are turned on. S14 provides studio CUT by grounding these resistors, and IC18 is a unity-gain buffer feeding the studio output EBOS. The studio output is not sent to patch, but emerges from the back of the LH PCB on a separate 4-pin connector.

The PFL-switcher allows the PFL or AFL signal, (in mono), to replace the normal CRM signal whenever a PFL/AFL condition is detected. Normally FET 1 is on, and FET 2 is off. A PFL/AFL condition reverses this, and the rest of the CRM chain is fed with either the PFL or AFL signal, selected by S8 and buffered

by IC6. Note that the studio feed is not disturbed as it is taken off just upstream of the switcher.

IC4A,B are the PFL and AFL summing amps, and IC5A,B invert the signals to maintain the phase. Direct PFL/AFL outputs are also available on a 4-pin connector on the rear of the PCB.

The CRM signal leaves the PFL-switcher and enters the mono/DIM network. S3 gives a mono check when closed as the signals are passively combined by R146, R175. Closing S1 shunts these resistors with VR2 and R199,200, giving a DIM drop variable between 3 and 20dB. A DIM condition is also automatically enforced when the talkback system is in use, and this is a quite separate facility fixed at 20dB attenuation; in use FET 4,FET 8 turn on and shunt most of the CRM signal to ground via R148, R179. A similar 20dB drop is enforced when the 'LISTEN TO CRM' facility is in use, as the listen signal is injected into the CRM path via low resistor R147.

The CRM signal now passes through IC16A, and the two CRM cut switches, S2A, (cuts both), and S5, (cuts right only). S4A selects the CRM signal to either main or alternate outputs, and IC17A,IC19A are the respective post-amps, cancelling out the inversion given by IC16A. The feeds then pass through an EBOS, and the to a 4-pin connector.

The Phones 1 select matrix allows a headphone feed to be made up from any combination of aux master signals, plus the CRM stereo signal. Resistors R65 to R84 are used for passive mixing, so that when more signals are switched in, the gain for any one signal drops. Aux master feeds can be switched in as stereo pairs, (1-2,3-4,5-6), or as single mono feeds to both left and right phones channels. Unused input resistors are grounded by the switch back-contacts to minimise crosstalk. Two 22K resistors are permanently connected for the injection of talkback.

VR5 acts as the phones level control, and the signal level is restored after the passive mixing by IC8A, with gain defined by R86,87. From here the signal goes to a standard EBOS circuit.

The SIP/PFL/AFL detection system uses IC7A,B as comparators to determine which of its three states the solo-enable, (SEN), bus is in. When the bus is midway between logic high, (-10V), and logic low, (-22V), both comparator outputs are low, indicating that the system is inactive. Comparator thresholds are defined by R41-R44. C13 slows the bus edges slightly, to prevent crosstalk of clicks, and R40 defines the voltage of the SEN bus midway when nothing else is connected to it. R45 ensures correct comparator operation in the face of large common-mode voltages.

In SIP mode, the SEN bus is taken high through a 100K resistor, and IC7B output swings high. If the SIP enable switch S7A is operated, this high is passed on to the solo mute, (SMT), bus

via R55. Q6 is an emitter-follower to drive the SMT bus, and R16,C16 slow the voltage edges. R59 ensures Q6 is off when S7A is not operated, and D7 allows the RED LIGHT facility, (RH Command PCB), to disable the SIP system by holding Q6 off. In SIP mode S7B opens, and Q4 is held off via D12, illuminating LED 1 steadily, to alert the user to the fact that a destructive SIP mode is ready. When a SIP is actually detected, D12 is reverse biased as IC7B output goes high, and the base drive for Q4 is now provided from the 2Hz sine oscillator via R193,190 causing LED 1 to flash, indicating that a SIP is actually happening.

In a PFL/AFL mode, the SEN bus is taken down to -22V via a 1K resistor, ensuring that any SIP condition will be overridden. In this case the output of IC7A goes high, and that of IC7B remains low. FET drivers Q2,Q3, now change state, causing the PFL switcher to route the PFL/AFL signal to the monitors. Q2 drives Q3 via R49, and also LED controller Q5 via R191; in PFL mode Q2 collector goes low, Q3 collector goes high, and Q5 is now dependent on R192 for its base drive, which comes from the 2Hz oscillator. This causes LED 2 to flash in PFL modes.

To summarise the LED operation, the SIP LED may be OFF, (SIP system safed), steady, (ready for SIP), or FLASHING, (SIP actually taking place.). The PFL LED may only be OFF, (no PFL buttons pressed - normal operation), or FLASHING, (PFL mode taking place).

The 2Hz (VLF) oscillator generates a slow sinewave to drive the mixer flash bus. A sinewave is used for this as any waveform with edges would be liable to crosstalk into signal circuitry. The oscillator is in two halves - a bandpass filter IC12A, which defines the frequency of oscillation, and a soft clipping amplifier IC12B, which regulates amplitude. Both stages are inverting, giving the overall positive feedback required for oscillation. A sinewave leaves the bandpass filter, undergoes mild clipping, and is fed back to the filter, where the harmonics introduced by clipping are removed. Bias network R195,196 causes the oscillator output to swing about the midway point of the CMOS logic range, in conjunction with zener D17, which gives a voltage shift downwards.

The switch tuned oscillator is built around IC1,2,3. The heart of the oscillator is the state-variable bandpass filter, consisting of two integrators, (IC1B,IC2A), and adder/subtractor IC1A. This filter defines the oscillation frequency, being tuned by varying the input resistors to the integrators; these are switched in and out by the switch-bank on the oscillator sub-PCB, connected via Conn 32.

The amplitude of oscillation is controlled by R4,5 and the associated diode-transistor network. This network acts as a sort of soft zener-diode; when the signal across R6,7 becomes great enough, Q1 turns on, increasing the amount of negative feedback applied to IC1A non-inverting input, and reducing oscillation amplitude. D1 to D4 are simply a bridge

rectifier to make the circuit work for both polarities.

The oscillator is disabled by S26A, the OFF switch, which opens when pressed, or by F9 turning off under the control of the RH Command PCB. Either operation increases the negative feedback to IC1A to 100%, and stops oscillation gently.

From the state-variable output, the oscillator signal passes through C3, and, if the SINE switch is in, goes through low-pass network R9,C5, which compensates for the tendency of the oscillator to increase in amplitude at the top of its frequency range, to level control VR6. If SQR or PULSE are in, the signal is taken from the comparator stage IC2B. In SQR mode the comparator threshold, (on the inverting input), is set at 0V to give zero-crossing detection, while in PULSE mode a bias from R14,15 is applied to give an asymmetrical output. Note that in sine mode the threshold is set to the negative rail by R11 to disable the comparator. R12 gives a very small amount of positive feedback to speed-up switching, and R13 renders SQUARE and SINE peak amplitudes the same.

IC3 is a conventional gain-stage that also provides enough current to drive the bus slating resistors. S29 controls the oscillator feed to the Aux buses, and EBOS 10 provides a balanced feed of oscillator signal. S33 selects this balanced output to the patch, and S32 brings in a balanced 40dB pad so that mic inputs may be tested. S30, (24-TRK), lets the oscillator unbalanced signal through to the group bus slating resistors on the RH PCB, and F10 allows this path to be interrupted by the RED LIGHT facility.

IMPORTANT: Note that while the RH Command PCB may be operated and to a large extent tested without the LH Command PCB, the reverse is not true, as the LH PCB relies on the RH PCB for logic power rails and FET drive signals.

7.05 RH Command PCB description

The right-hand command PCB is described in the following order:-

Aux master circuitry

Talkback, listen, and oscillator signal routing circuits

Command logic

Each Aux master consists of a discrete/op-amp, a level-control post-amp, and an electronically balanced output stage, (EBOS). Each of the 6 aux masters drives both Phones Matrix 1 and 2 and also a PFL/AFL facility. All six are identical, and only Aux 1 will be described below. Note that for Aux 2 the resistor the corresponds with R112 will be R122, that for Aux 3 will be R132, and so on. A similar scheme is used to identify the other components.

The aux sum amps are substantially identical to those described under the heading of the LH Command PCB, but the feedback resistors, (R112etc), are of a higher value, to allow the stage to give a 4dB gain when used with the 7K5 mix resistors on the I/O module. Note that R170,C95 and R171,C96 decouple the supply rails for all six aux master sum amps.

From the sum amp the aux signal passes through a level control VR1, and then to the post-amp stage IC15a, which is configured for a gain of 10dB. From here the signal passes to the EBOS, which is identical to that described for the I/O module, and to PFL/AFL switch S1. Note that although both PFL and AFL buses are driven, both receive an after-fade signal. The other half of S1 removes a short across LED 1 when operated, giving an indication that PFL/AFL is active. Whenever one or more of the LEDs in the ladder, driven by R69, is on, Q29 is turned on by the LEDs forward voltage, via R70, and pulls down the SEN bus via R183, to assert a PFL/AFL condition. As usual, this overrides any SIP condition that may exist.

The phones matrix operates exactly as described for the LH Command PCB; VR9 is the level control, IC11 the post-amp, and EBOS EB6,7 provide balanced outputs. Talkback is injected into the matrix through R79,80.

The talkback signal originates from the familiar type of electret microphone. Its internal pre-amp is powered via R72,C14, and the output from this further amplified by IC9a. This stage has a variable gain set by VR8, and maximum gain set by R75. The talkback signal, (from here on referred to as TB), may be routed to the phones matrix OR the aux buses directly, (this link is selectable), by F3. This is controlled, via the command logic, by the TALK TO PHONES push button. When F3 is off, F8 is on, to ensure that no trace of signal passes through when not required. Similarly, F4,F10 control the TB to the studio signal path, and are activated by the TALK TO STUDIO button.

The TALK TO ALL button activates TALK TO PHONES also, (but not TALK TO STUDIO), but its main function is to route the TB signal, mixed with a low-level 30Hz slate tone, to all 24 group buses. The 30Hz tone is generated by oscillator IC10a, which can be regarded as a simple form of Wien-bridge. R89,90,C32,33 set the frequency and D25,26 regulate the amplitude. F7 disables the oscillator when it switches off as this results in 100% negative feedback. The 30Hz tone is mixed with the TB signal by IC10b, and this can then be routed to group buses and the mix bus by F2 and F1 respectively. The resistors feeding the group buses are in DIL packages DIL 1,2,3. F9 is on when F1 is off, to ensure that nothing unwanted reaches the mix bus, and F6 performs the same function for F2, F5, and the oscillator disable FET on the LH Command PCB.

The listen microphone is external, presumably in the studio, and feeds a standard balanced input stage built around Q30,31 and IC9b. The listen signal, hereafter called LSN, may be routed to the group buses by means of the LISTEN TO TAPE switch, which turns on F5, and for this it uses the same DIL resistor array as TB. The logic ensures that F6 turns off as required.

The other LSN function is activated by LISTEN TO CRM, which, as previously described, routes the LSN signal to the CRM path via FETs on the LH Command PCB.

RH COMMAND LOGIC PCB

The command logic is inevitably complex, but may be broken down as follows:-

- Master status logic: ie MIX/REC, GRP/TAPE
- Talkback signal control
- Listen mic signal control
- RED LIGHT system to render ancillaries safe for recording
- Programmable mute bus control

This last function is essentially separate from all the others, but the rest are interlocked to some extent.

The master status logic issues the central commands to set the REC/MIX mode in each I/O module, (basically EQ in channel or mix), and likewise GRP/TAPE mix path source switching. No matter what local flips have been established, a central command will pull all I/O modules to the same state. Note that the facility also exists to command the TV mode from this point. The central logic also assumes responsibility for initial reset of these two parts of the local I/O logic.

Two safety features are provided to prevent hasty button-presses from clearing a desk-full of carefully preset local flips, and also to minimise the possibility of this disrupting recording. The most important is RED LIGHT, which disables the other sub-systems such as the line-up oscillator. Another press of RED LIGHT is required to free the master status buttons.

A secondary precaution is the STATUS, (unlock), button, which must be pressed before the REC/MIX mode can be changed. This works on a time-out basis, giving approx 10 seconds to change status before it resets itself. The GRP/TAPE master buttons are not affected by this.

It is now necessary to delve into the details of the logic; this is a combination of CMOS and discrete diode-transistor circuitry.

The master GROUP/TAPE status for the console is stored in flip-flop IC1c,d. The output of IC1d goes high to indicate TAPE mode, and illuminates L1 via lamp-driver Q1 to display this, (only one lamp-driver circuit is shown, the rest are identical.). Likewise, the output of IC1c goes high to indicate GROUP mode, and vice-versa. This output drives the lamp L2 in the GROUP switch.

The flip-flop state is changed via the GROUP and TAPE buttons, which pull down inputs on the gates; the inputs are normally held high by pull-up resistors R29,30. However, when the logic signal not-RED LIGHT, (hereafter shortened to not-RL), is low, ie a RED LIGHT condition does exist, analogue gates IC3b,c are switched off and the GROUP/TAPE switches are disabled. Gate IC3a defines priority when both GROUP and TAPE are pressed at the same time; the TAPE signal goes low, turns off IC3a, and prevents the GROUP low from reaching the flip-flop.

The GROUP and TAPE master signals are sent out along their control buses as low-going pulses, rather than a DC level, to simplify I/O module circuitry. This is done by simply sending out via the IC2 gates, (which increase the drive capability), the flip-flop triggering signals. The only function of the flip-flop is to provide latching for lamp-indication of status. The outgoing pulses are smoothed slightly by R37,C1 and R38,C2 to eliminate crosstalk clicks.

The GROUP/TAPE status is required to follow the REC/MIX status, such that pressing RECORD will enforce GROUP, via D2, and pressing MIX will enforce TAPE, via D1. TV mode enforces TAPE mode, via D10 and then D1. Initial-reset of the GROUP/TAPE flip-flop is also done through these diodes, when the REC/MIX circuitry is reset.

The main console status, (RECORD, MIX, or TV), is stored in two CMOS flip-flops, built from IC1a,b and IC4c,d. (See diagram). Each of these is set by its associated push-button, set meaning that the output of the first gate in the flip-flop pair goes high to assert its mode. Pressing REC to enter RECORD mode takes both of these outputs low.

To simplify the I/O logic, the REC/MIX status is sent out as a DC level via R170, (and slightly smoothed by C98), such that logic high represents MIX, and low is RECORD. Also a CHANGE signal is sent out via R39,C3, pulsing high to indicate that

a mode change is occurring, and telling the I/O module logic to update its state.

The REC/MIX flip-flop IC1c,d is set and reset as before by logic lows applied against pull-up resistors R31,32. As before, IC3d sets priority, so that if REC and MIX are pressed together, the MIX low turns off IC3d and the REC signal is blocked. Lamp drivers using Q3,Q4 display the flip-flop state.

The CHANGE signal is generated by D6,7,8,9, which pull R36 low when either REC, MIX or TV is pressed; this low-going pulse is then inverted by IC4a before being sent out. D6,7 also generate a low-going pulse only when either MIX or REC are pressed; this resets the TV-mode flip-flop IC4c,d via pin 13. Similarly, pressing TV resets the REC/MIX flip-flop to MIX via D10.

The initial state of the console on power-up may be set by a link to be REC, MIX, or TV, with GROUP/TAPE following as normal. This is done by C4, which generates a low-going pulse on power-up and applies it to the appropriate flip-flop gate via the programming link. D4 prevents button-presses giving spurious resets.

As stated above, the REC, MIX and TV buttons are only enabled when the STATUS unlock button has been recently pressed, and is illuminated. Normally C5 is kept charged to a logic high by R38. This keeps the output of IC4b low, leaving Q15 off and the lamp L6 out. While Q15 is off the master-mode buttons cannot generate a logic low and are therefore disabled. Pressing STATUS discharges C5 via current-limit resistor R39, and the output of IC4b remains high, enabling the buttons, until C5 slowly charges again. The status-unlocked period may be prematurely ended by a RED LIGHT condition, which quickly charges C5 through D11.

RED LIGHT is a safety condition which disables any console facility that could accidentally disrupt recording, eg slating the talkback mic to groups instead of Phones mix.

The functions of RED LIGHT are as follows:-

- 1 Disable GROUP/TAPE buttons.
- 2 Disable REC/MIX/TV buttons by resetting STATUS.
- 3 Disable Solo-In-Place mute bus, (SMT).
- 4 Disable Line-up oscillator, and switch off its output.
- 5 Disable LSN and TB feeds to slate resistor array.
- 6 Ground slate resistor array.
- 7 Reset LSN TO CRM flip-flop.
- 8 Signal RED LIGHT condition to external equipment.

In the explanation that follows two main logic signals occur. RL represents RED LIGHT, and is high when the condition exists. Its complement, not-RL, is low when the condition is true; this inverted signal is represented on the circuit diagram in the usual way, with a bar over RL.

RED LIGHT is controlled by a flip-flop toggled by the usual illuminated push-button. The flip-flop is made from NAND gates IC5a,b. This works in exactly the same way as the flip-flops on the I/O module. (qv) C10 holds a charge which can only momentarily overpower the latching positive-feedback through R40, when ever the button is pressed. On power-up the RED LIGHT is reset, (ie RL low), via Pin 1 on IC5a. In this state the button lamp L7 is off and Pin 3 is high.

The signal leaving IC5a is combined with a possible external RED LIGHT signal by IC5c. Either an outside signal, (power applied via R67 turns on the phototransistor in IC19a, pulling down Pin8), or a set flip-flop will give a RED LIGHT condition. Note that the button Lamp-driver Q7 also drives the other half of the opto-isolator, (IC19b), via R45 to signal RED LIGHT to the outside world. D12 prevents the lamp keep-warm current, set by R14, from turning on the opto LED.

The output of IC5c is the RL signal, and IC5d inverts this to give not-RL. The RL signal performs the following functions:-

- a. Resets the STATUS-unlock timer via D11.
- b. Turns on Q17, the FET driver that, by turning off FET9 on the LH Command PCB, disables the oscillator.
- c. Turns on Q18, which turns off FET10 on the LH Command PCB, blocking the oscillator output path.

The not-RL signal does the following:-

- a. Locks out the GROUP/TAPE buttons by turning off analogue gates IC3b,c.
- b. Forces Q16 off by shunting away its base-drive via D33. This ensures that the slate-resistor DIL array is grounded at its input by FET6.
- c. Resets the LISTEN TO CRM flip-flop via D14.
- d. Disables the LISTEN TO TAPE, TALK TO ALL, and TALK TO STUDIO switches by preventing them generating a logic high, as not-RL has gone low. See Pin 4 of Conn 2 to the status switch PCB.

There remains three groups of switches to describe. The two LISTEN buttons, the three TALKBACK buttons, and the two master mutes A,B. The master mutes form a separate function group, but the LISTEN and TALKBACK functions are interlocked with the line-up oscillator, to ensure that only one of these can access the slate-resistor array at one time.

The priorities are arranged as follows:-

1. LISTEN disables line-up oscillator.
2. TALKBACK disables LISTEN and line-up osc.
3. RED LIGHT disables all three, as described above.

The LISTEN TO CRM function is controlled by a flip-flop built from NAND-gates IC6c,d with storage capacitor C11. The flip-flop can be reset on power-up via D15, and by RED LIGHT via D14. Lamp-driver Q8 indicates its state. When the flip-flop is set, (ie lamp L8 on), Pin11 of IC6 goes low, turning off driver Q24, and turning on the FETs on the LH Command PCB that inject the LISTEN signal into the CRM path.

The LISTEN TO TAPE function has a momentary push-button action, indicated directly via lamp-driver Q9. Its purpose is to route the output of the LISTEN mic amp to all 24 groups, via the slate-resistor array. This is done by turning on FET5 and turning off FET6. Pin 1 of IC6 is normally high, so the high applied to Pin 1 takes the output low, turning Q21 off, and turning on FET5, which is driven from Q5 collector. Q16 is turned on via D32,R189 and R190, turning FET6 off.

Note that LISTEN TO TAPE overrides line-up oscillator, as D17 turns on Q18, which turns off FET10 on the LH Command PCB, blocking the oscillators path to the slate array.

TALK TO ALL routes the talkback, (TB), signal to all groups via the slate array, to the MIX bus via separate slate resistors, and also activates the TALK TO PHONES function, which is described later. A low-level 30Hz tone is added to the TB signal.

TALK TO ALL is a momentary action function, the push-button generating a high that turns on Lamp 10 via lamp-driver Q10. The fixed 20dB CRM dim is activated via D19, and TALK TO PHONES by D21. The line-up oscillator is disabled via D31, which turns on Q18, and blocks the oscillator output as described for LISTEN above. IC6b inverts the signal so that it is now active-low, and Q19 is turned off, turning on FETs 1,2. Q20 also turns on and turns off FET9. D30 turns on Q16 via R189,190, as for LISTEN. Finally FET7 is turned on via D16, which starts the 30Hz oscillator.

TALK TO STUDIO is also a momentary function. A 20dB CRM dim is asserted via D18, and IC7b inverts the logic signal to active-low, turning off Q22 and turning on Q38. These turn on FET4 and off FET10, respectively. The TB signal, (without 30Hz being added), is then routed to the studio path.

TALK TO PHONES is another momentary function, monitored by Q12, driving lamp 12. D20 asserts a 20dB fixed CRM dim, and the inputs to IC7d are pulled up via D22, its output going low. Q25 turns off, and Q28 turns on. This turns on FET3, and turns off FET8. Note that IC7a is not used.

Master mutes A and B are both controlled by standard flip-flops built from IC8a,b and IC8c,d respectively. To assert a mute, the relevant control line is pulled low by Q26 or Q27. The flip-flops reset to the unmute condition on power-up via Pins 1 and 13.

All logic on this PCB is powered from a 78L12 IC regulator IC18. The ground of this is referenced to the -22V rail, so that a logic low is -22V, and a logic high about -11V, when using a ground-referenced voltmeter. Referencing it to -22V is usually less confusing.

7.06 TS24 Metering System Circuit Description

This description covers the TS24 VU/Peak LED-bargraph metering system. This consists mainly of the LED display PCBs, each holding 8 bargraphs, and 8 rectifier sub-PCBs.

<u>Name</u>	<u>PCB No.</u>	<u>DRG No.</u>
TS24 Meter Rectifier PCB	SC1553	ED2198
TS24 LED Display PCB	SC1399	ED2186

NB. Early TS24 models were fitted with an earlier model Rectifier PCB (SC1398) not fitted with a Peak-drop trim pot.

Meter Rectifier PCB

This card takes a signal input, and converts it into a DC voltage that is used to control the bargraph circuitry. The card operates in either VU or Peak mode, determined by a logic control line activated from the master metering section. This is high for VU, and low for Peak; +7.5V and -7.5V respectively.

The input signal comes in via unity-gain differential input amp IC1a; this in fact receives a single-ended signal from a TS24 module, with a nominal level of -2dBu. The output of IC1a passes through VU calibration preset PR1, which is normally set to illuminate the first red LED, (=0VU), at a level of -2dBu. The signal from the preset wiper is then amplified to a suitable level for further processing by IC1b, with gain set by R22, R5 only, as in VU mode IC3a is off. (The differences in Peak mode will be dealt with later).

IC2a,b make up a precision full-wave-rectifier circuit that gives a positive output only. IC2a is a precision half-wave rectifier; on positive half-cycles of the input D2 conducts and an inverted replica of the input wave-form is produced by R6,7. On negative half-cycles D2 is off and D1 conducts, so that the op-amp inverting input remains at virtual earth and there is no output. The output half-cycles are summed with the original signal at half the level, by IC2b, and the result is positive full-wave rectification.

In VU mode, IC3b is off and IC3c is on, so that the rectified signal is averaged by R14,C3, to give VU characteristics. The resulting DC is amplified with a gain of 2 by IC2d, and passed out to the LED bargraph comparators.

In Peak mode, the gain of the amplifier IC1b must be reduced, as the peak value of a signal is usually higher than its average. A sine wave has a peak value approx 3dB higher than its average, and so to obtain the same reading the gain would have to be reduced by this amount. Music signals are normally a good deal peakier than this, and so provision for more gain reduction is needed; for the TS24 8dB is standard. This peak-mode drop is set by PR2, the range available being 3 to 13dB.

Peak-mode is signalled by the CTRL signal going low. IC3d switches off, Pin 11 goes high, and IC3a switches on, providing extra negative-feedback and reducing the gain.

Simultaneously, IC3c turns off, and IC3b turns on, allowing C3 to be charged by the active peak-detector IC2c, which operates similarly to IC2a, with R12 defining attack time. Normally the charge on C3 decays through R11, but this is delayed for a fraction of a second to give a momentary peak-hold, making brief transients more visible. This is done by Q1, which is held off for a moment after a peak has been detected by the charge stored on C2, which discharges through R13.

LED Display PCB

This PCB holds 8 modules worth of LED bargraphs, and each consists of 3 LED arrays and 3 LM3914 multiple-comparator ICs. Virtually all the circuitry, (resistor ladders, comparators, and LED drivers), are within ICs, and it is only necessary to note that LED brightness is set by R4,5,6 and D1 is required to drop the +24V rail down to about +18V, suitable for the 3914s.

A quasi-logarithmic law is provided by causing the voltage set at the top of the resistor ladder to be increased as the input DC voltage increases; this is done by R2 and R3.

Calibration

Calibration is normally done by setting the VU sensitivity first; the first red LED segment illuminating at an input to the metering system of -2dBu. (=0VU). Note that this corresponds to an output from the balanced O/P stage on the I/O module of +4dBu.

The sensitivity drop on entering peak mode is set to -8dB, though the available range is -3 to -13dB.

TS24 PHASE METER CIRCUIT DESCRIPTION

This description covers the TS24 MIX VU and phase-meter drive card, and phase-meter LED display card. The drive card also generates the VU/PK control signal for the main metering system.

	PCB No	DRG No
TS24 VU and phase drive PCB	SC1534	
TS24 Phase LED Display PCB	SC1535	

VU & Phase Meter Drive PCB SC1534

This card takes two signal inputs, (the CRM/PFL L and R signals), and generates VU-meter drive signals and also converts the average phase difference between the two inputs into a DC voltage that is used to control the phase-meter bargraph circuitry. The card also generates the CTRL signal to determine if the main metering system operates in either VU or Peak mode. This CTRL line is high for VU, and low for Peak; +7.5V and -7.5V respectively.

The input signals come in via variable gain differential input amps ICa,b; these, in fact, receive single-ended signals from the TS24 Command module, with a nominal level of -2dBu.

Gain adjustment is by VR1,VR2, which control the amount of negative feedback through R5,11. R4,10 maintain DC feedback to the op-amps. The VU meter drive signals are taken directly from the op-amp output signals.

The two signals next enter clipping stages IC2a,b which convert the input into a square wave of peak voltage +/- 0.6V. This occurs as the negative feedback to IC2a,b is via the back-to-back diodes. The bias resistors R14,20 ensure that the output is hard over and not dithering about or oscillating in the absence of any significant input. The low amplitude square wave is then amplified by IC2c,d, level shifted by R17,18 and R23,24, and further sharpened up by IC3c,d. This makes the signal suitable for application to CMOS Exclusive-Or gate IC3b, which is powered from the 0V and +7.5V supply rails. This EXOR gate acts as a phase-detector, as its output is only low when the inputs are the same, ie both high or both low. This signal is then inverted by IC3a, and integrated by R25,26 and C7. Therefore the output voltage on CONN Pin 1 is reduced as the average phase difference between L and R increases.

The Peak/VU toggle circuit is made up of IC4a,b. Normally positive feedback through R27 holds the flip-flop in a stable state, but when the push-button connected between pins 2 and 3, (CONN 3), is closed, the opposite logic-level stored on C8 overpowers R27 and reverses the state. However, R28 is too high in value to accomplish this by itself, and so the push-button must be released for a while so that C8 can have its charge reversed via R28. TR1 controls the Peak/VU indication lamp built into the push button.